SECTION 2
EWS SCHEMATIC RULES AND GUIDELINES
Q20000 (210)

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1 EWS Schematic Rules and Guidelines

1.1 EWS and Netlist Submissions

The following rules are generic and apply to all schematics captured on any engineering workstation (EWS) such as a DAZIX, Mentor or Valid, or any other system used to generate an AMCC-readable netlist for submission to AMCC.

For EWS-specific schematic rules and procedures, refer to Volume II. of this design manual This volume contains software user's guides, ***EWS Schematic Rules and Guidelines*** (this document) and ***Vector Rules and Guidelines.***

1.2 Copies

- AMCC must be provided with copies of the customer's logic diagrams, blueprints or schematics, one of which is marked to show the critical and performance-sensitive paths, including paths to be tested with AC Test vectors.

  For EWS-based designs, send two (2) hardcopies

  For non-EWS-based designs, send three (3) hardcopies

- A block diagram should be included with the schematics. If hierarchical EWS schematic capture is done, the block diagram is an integral part of the schematic set. In this case, refer to "Hierarchical Design - Rules" in this document.

1.3 Schematic Border

- Schematics must be labeled with the following:

Company name	Circuit name
AMCC circuit name	PO # (if known)
AMCC array	Designer's name
Date	Page number
Revision level	

- Use an AMCC border on all EWS schematic pages. Fill in via notes the page description, designer, date, page number and revision level, etc. as indicated above.
- All schematics should be freely, extensively commented for clarity
- Mentor EWS: If a different border is required consult Volume II for instructions and consult AMCC. Documentation on the border will be required to be in the design submission package. The border must also be submitted on electronic media.
- All pages must be commented with a page number within the border, and all page numbers should be sequential. The last page should be clearly identified, (e.g., page 10 of 10).
- Follow the EWS-specific rules (in Volume II) regarding page names for hierarchical or nested EWS schematics. Also see "Hierarchical Design Rules" at the end of this section.

1.4 Chip Macro

Every circuit must use a chip macro. The chip macro identifies the specific array, ECL type, I/O mode, and provides the AMCC MacroMatrix ERC software with array-specific parameters. AMCC prefers that the chip macro be placed on page one of a design. Its location is page-independent to the software.

1.4.1 Chip Macro Parameters

The required chip macro parameters must be defined. Refer to the *AMCCERC User's Guide* for more detail.

- **product_name** Required; The AMCC-assigned name.
- **device_number** Required; The AMCC-assigned number.
- **product_grade** Required; **MIL** or **COM** for military or commercial. (Do not use COM4, COM5, MIL4 or MIL5.)
- **power_supply** This is an optional parameter. AMCC prefers that it be supplied. The value can be **STD4** (-4.5V), **STD5** (-5.2V) or **5VREF** (+5V) and applies to the ECL supply. It is included on all applicable chip macros.

1.4.2 Chip Macro Pins

- The chip macro input pin must be attached to the global ground. This procedure is EWS-specific. Refer to Volume II for the exact method of specifying that a pin is to be connected to "GROUND
- If power and ground need to be rotated, refer to Volume II for EWS-specific schematic rules and procedures.
- Chip macro output pins labeled Y must be terminated. Refer to Volume II for the EWS-specific method of terminating an output pin. (Refer to Volume I, Section 2 for an example chip macro, labeled and wired.)
- Bipolar chip macro output pins labeled VTA may be terminated, if not required by any BIxx macros. If BIxx macros with VTA inputs are used on the circuit, then the chip macro VTA output pin must be routed to these pins.

1.5 Cross-Coupled Gates

- Cross-coupled gates constructed to form latches are not allowed. Significant timing and reliability problems are created relative to min-max conditions. Each use must be approved by AMCC Implementation Engineering prior to submission.

1.6 Added Power and Ground

- When the number of power and ground pads needs to be increased due to simultaneously switching outputs, 3-state enable-drivers, or for added noise immunity, extra power and ground macros must be used.
- The extra power and ground macros must be individually placed on the schematics by the designer. Use macros ITPWR, ITGND, IEVCC.
- These macros must have instance (occurrence) names.
- AMCC prefers that all power and ground macros be placed with the circuit chip macro on page 1 of the schematics. Then start the design on page 2.
- Wire the power and ground macro inputs and outputs in the same manner as described for the chip macro. Inputs are tied to global ground and outputs are terminated.

For visual clarity, the wires should point up for all VCC supplies (GND for STD-REF ECL) and point down for all VEE supplies (GND for +5V REF ECL or +5V only circuits).

1.7 Signals, Pins and Connectors, Strange Macros and Miscellaneous Symbols

- Only AMCC-created macros (Mentor, DAZIX, Valid) and EWS-specific connectors and terminators (DAZIX, Valid) may be used on any EWS schematic. For Mentor, AMCC connectors and

terminators must be used (supplied with library).

- Only released AMCC macros may be used in a design. For custom logic, please consult AMCC.
- EWS system primitives may not appear on a schematic.
- All array I/O signals must use a primary input, primary output or primary bidirectional connector.
- *All on/off or inter-page signals must use page connectors with comments as to source page (for input), destination page (for output). Refer to Volume II.*
- *All intra-page signals (a signal broken up on the same page for clarity is an intra-page signal) must use connectors. Refer to Volume II. Minimize on-page breaks as they are hard to read.*
- The global ground symbol and the termination symbol should be shown on the schematics where pins are tied to global ground or are terminated.
- Rotation: the conventional logic flow on the page is from left (input) to right (output). AMCC prefers that rotation of macros and other schematic objects be kept to a minimum to maintain this flow convention.
- Spacing: All schematic objects (macros, connectors, terminators, blocks, cells, etc.) and wires and busses must be spaced at least two (2) grid positions apart, leaving enough room for a readable note to fit between them or for names to be properly placed.
- Do not overlap schematic objects, place on top of one another, or overcrowd so that they touch in any way. Only wires and busses may connect to schematic objects.
- Do not wire through schematic objects.
- The schematic must be human readable - logic should be functionally grouped on the same or sequential schematic page(s).

1.8 User-Defined Unique Names (Instance, Occurrence)

- All macros must be given user-defined unique names in a flat design. Follow EWS-specific naming rules for nested or hierarchical designs (refer to Volume II or the workstation manuals).
- All user-defined instance names are limited to a maximum of six (6) characters in length. Instance names are user-defined occurrence names of macros, cells, blocks, etc.
- All user-defined signal names are limited to a maximum of eight (8) characters in length.
- User-defined subscripted names, nested and hierarchy names, must follow the EWS-specific rules (Volume II or the workstation manuals).
- All user-defined names in a circuit must be composed of alphanumeric characters (A-Z, 0-9). Short, meaningful names are recommended.
- All user-defined names may begin with a letter or a number.
- User-defined names must NOT contain spaces or special characters.
- Do not use duplicate names, AMCC macro names, or connector names as unique signal or as unique instance names. All names must be unique within a circuit.
- Do not use keywords or reserved words as a name. Reserved words: See Volume III, ***AMCCERC User's Guide*** for the description of the Valid Name Check ERC.
- Grounds and terminators are not given user-defined names.
- Default names, those automatically generated by the EWS, are not allowed. Changes cause renaming of defaulted items and loss of continuity.

1.9 Naming Signals

The following signals must be given unique user-defined names:

- All off-chip signals; wires attached to I/O macro PAD pins and external connectors.

- All page-to-page (inter-page) signals; wires attached to page connectors.
- All on-page signals; wires attached to intra-page connectors.
- All 3-state enable control signals or bidirectional macro enable signals; wires attached to the enable pins.
- All signals in a critical path or in a path which will be examined by the at-speed simulation or AC test simulations.

1.10 Unused Internal Macro Input Pins (Non-Primary Inputs)

- Unless otherwise specified on a specific macro data sheet in Volume I, Section 6, Macro Library Documentation, all unused internal macro input pins must be attached to the global ground ("GROUND" for all bipolar, BiCMOS I/O; "VDD" (HIGH) or "VSS" (LOW) for internal BiCMOS).
- This procedure is EWS-specific. Refer to Volume II for the exact method of specifying that a pin is to be connected to "GROUND", "VDD", or "VSS".
- **Bipolar**: Exceptions to the preceeding rules are those macros with pin hook-up restrictions. Be certain that all macro input pins that must be driven by a macro are so driven and are not tied to "GROUND". In cases where an invariant signal is desired, buffer-driver macros may be used to drive from 32 up to 50 static loads, depending on the series.

1.10.1 Q20000 Series:

- For 1-18 loads: Use a simple L-option OR/NOR gate macro
- For 18-50 loads: Use the static driver (HI/LO) macro.

1.11 Unused Internal Macro Output Pins (Non-Primary Outputs)

- All unused internal macro output pins must be terminated.

1.12 Simultaneously Switching Outputs SWGROUP *- macro parameter*

- All simultaneously switching outputs must be tagged with the **switching group macro parameter, SWGROUP**. This will allow a correct I/O list to be generated and enable power/ground ERC checking.
- Refer to Volume II for EWS-specific information on how to attach the parameter and to the ***AMCCERC User's Guide*** for its use in the ***amccerc.lst*** and ***amccio.lst***. The parameter value must be visible on the schematic and may be assigned any alphameric string up to 8 characters.

1.13 Fan-Out Load Derating FOD *- net parameter*

- Fan-out load limits for all clock, timing and distortion-sensitive paths that are to be derated must use the **fan-out derating net parameter, FOD**. Refer to Volume II for EWS-specific instructions on how to attach the parameter and for its use in the ***amccerc*** Fan-out Check. The parameter value must be visible on the schematic and may be assigned any numerical value from 00 to 99.

1.14 Parametric Gate Tree Output GTO *- net parameter*

- If a parametric gate tree structure is being used to allow parametric testing, the **gate tree output net parameter GTO** must be attached to the primary output signal of the tree. Refer to Volume II for EWS-specific instructions on how to attach the parameter and for its use in ***amccvrc***. The GTO parameter value must be visible on the schematic and may be assigned any alphameric string of up to 8 characters.

1.15 Required Labeling of Critial Paths

- Critical paths should be clearly identified on the schematics via notes. AMCC requires that one set of schematics be marked, with a highlighter or pen, to show all critical paths that will be examined during timing verification.

1.16 Hierarchical Design - Rules

- No primary input, output or bidirectional macros, 3-state or bidirectional enable drivers may be sized, nested, or placed within a block, cell, frame or other sub-structure. They must appear on the top-level of the hierarchical schematics (first design page).
- The 3-state enable drivers that reside on I/O cells (bipolar) or macros on internal cells that directly drive the enable pins of 3-state TTL output macros or bidirectional macros (BiCMOS, Q20000 Series) must be on the top-level of the schematic.
- Added power and ground macros are considered primary inputs and must reside on the top level of the schematic.
- Do not use cells, frames, or sizing for internal logic elements that will require manual placement, net balancing or net matching. These elements and nets must be given user-defined names.

1.17 Verilog Schematic-less Submissions

- For Verilog designs to be submitted without schematics, consult AMCC. Refer also to the AMCC Verilog Design Manual.